A Specification Methodology by a Collection of Compact Properties

as Applied to the Intel® Itanium™ Processor Bus Protocol

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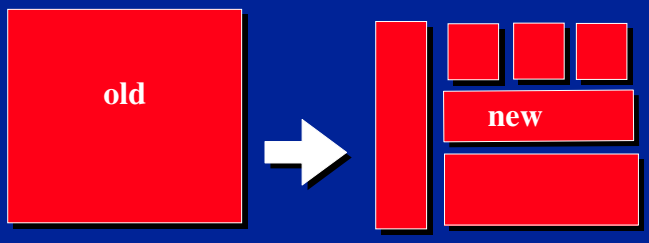
Stanford University
Intel® Corporation

Background

As digital circuit designs become more complex…



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Background

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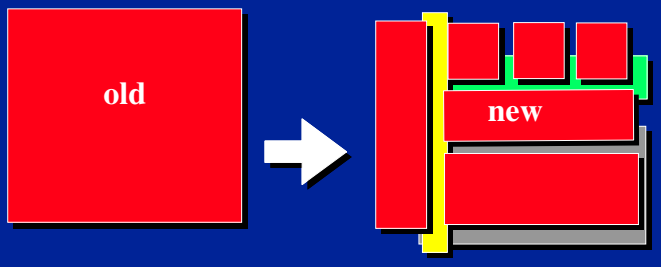

Interfaces must be clearly defined.

- Avoid communication problems between designers, IP buyer and seller, …

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Background

Problem

Target subsequent latency is the number of clocks from the assertion of IRDY# and TRDY# for one data phase to the assertion of TRDY# or STOP# for the next data phase in a burst transfer. The target is required to complete a subsequent data phase within eight clocks from the completion of the previous data phase. This requires the target to complete the data phase either by transferring data (TRDY# asserted), by

Current State

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Background

Problem

Target subsequent latency is the number of clocks from the assertion of IRDY# and TRDY# for one data phase to the assertion of TRDY# or STOP# for the next data phase in a burst transfer. The target is required to complete a subsequent data phase within eight clocks from the completion of the previous data phase. This requires the target to complete the data phase either by transferring data (TRDY# asserted), by

```
prev(!final_dphase_done & !idle)
        IMPLIES cbe_e;
prev(frame) IMPLIES (frame | irdy);
prev(stop & irdy) IMPLIES !stop;
prev(stop & irdy) IMPLIES !irdy;
prev(!frame) IMPLIES (frame | ad);
prev((counter = 3) & a) IMPLIES !a;
prev((m_initial = 7) & !irdy)
        IMPLIES irdy;
prev((m_subseq =7) & !irdy)
        IMPLIES irdy;
```

Current State

Why not this?

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Background

Goal

- **The cost-value problem**
  - **Too much time and expertise needed**
  - **Not very valuable**
- **Two-pronged solution**
  - **Make the specification process *easier***
  - **increase the *usefulness* of formal documents**

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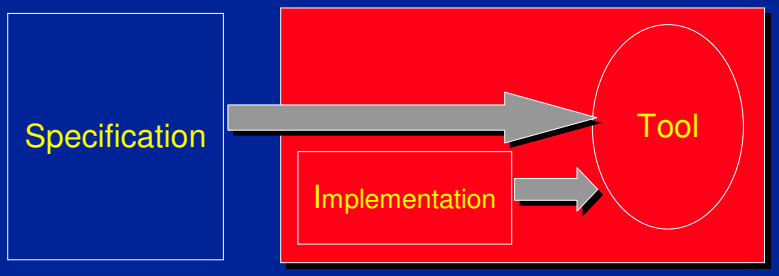
Background

Goal

- *Methodology* is the key
  - As opposed to *tool* or *language* development
- Little work on methodology so far



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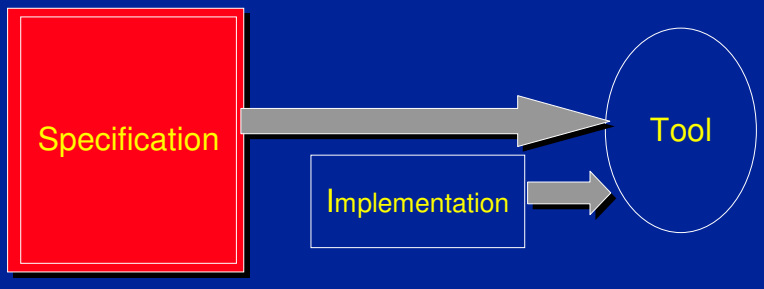

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Background

- In [SDH00] (Shimizu, Dill, Hu, FMCAD '00)
  - Using PCI as an example
  - Specification style developed
  - Two specification debugging methods described

Methodology

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Contribution

- Shows the method applies to more advanced bus protocols
  - Intel® Itanium™ Processor bus protocol
  - Example : pipelining
- Reports interesting issues revealed during the protocol development
  - Worked with Intel® to prepare a standard

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Outline

1. Methodology
2. Specifying the Itanium™ processor bus protocol
3. Checking the protocol

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Methodology

1.Monitor-Based Specification

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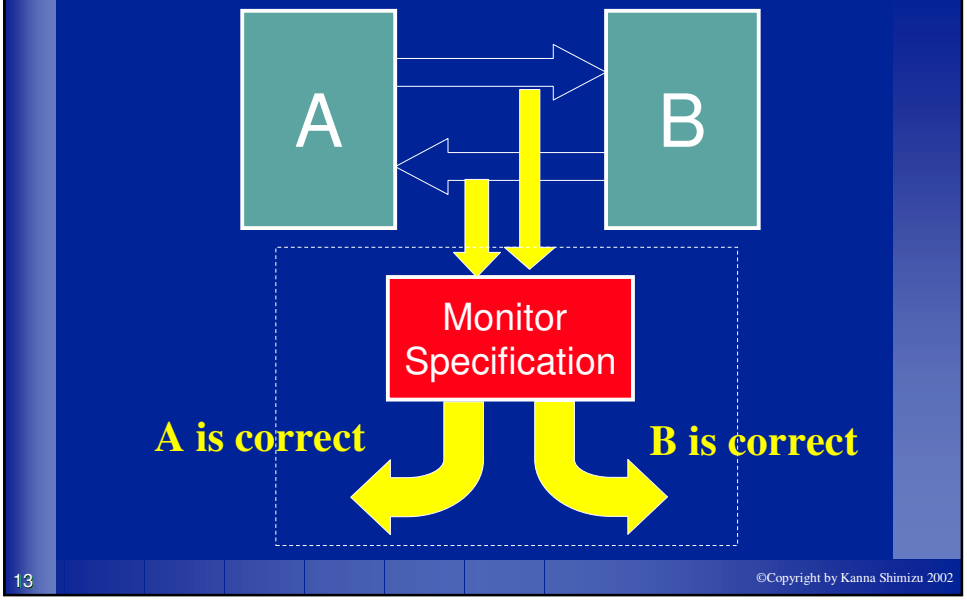
Methodology

Specification (1)



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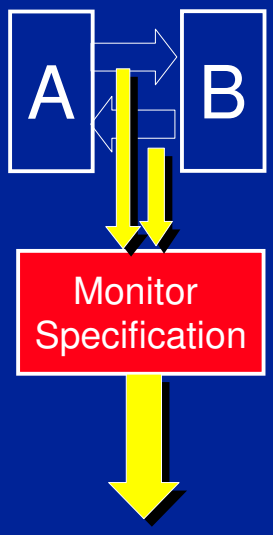
Methodology

Specification (1)



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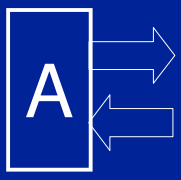
Methodology

Specification (1)



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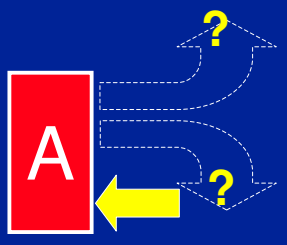
Methodology

Specification (1)



Generator
Specification

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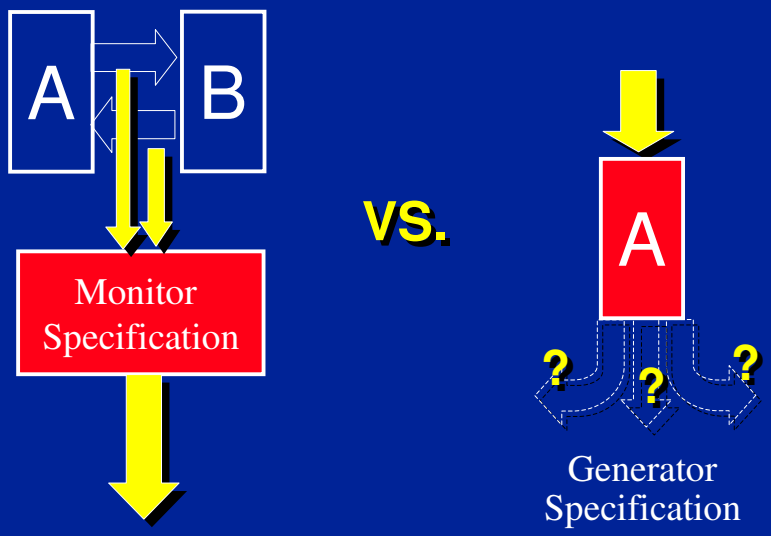
Methodology

Specification (1)



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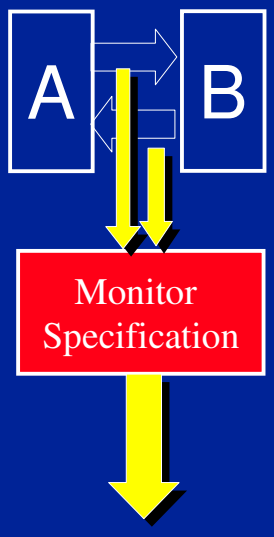
Methodology

Specification (1)



1. Monitor specification is deterministic
   - even if behaviour specified is non-deterministic
2. A list of simple constraints

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Methodology

2.Collection of Compact Properties

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Methodology

Specification (2)

Specify using a conjunction of simple constraints

prev(input0 & input1 & … | output0) IMPLIES

current(output1 | output2 & … & outputn)

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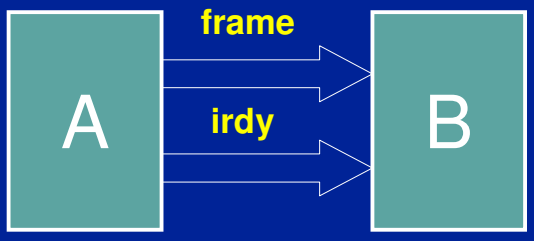
Methodology

Specification (2)

Example

"Only when IRDY# is asserted can FRAME# be deasserted"

prev(frame) IMPLIES frame | irdy



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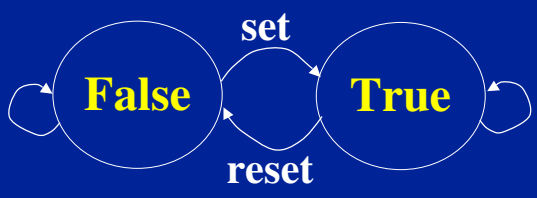
Methodology

Specification (2)

- Simple state machines each track one thread of information
- Use many *generic* state machines instead of a few custom ones
  - Example : set-and-reset state machine



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Methodology

Summary

The specification *style* requires

1. Observe; then, deem actions "correct" or "incorrect"
2. Many small properties and many generic state machines

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Outline

1. Methodology
2. Specifying the Itanium™ processor bus protocol
3. Checking the protocol

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Itanium™

Pipelining

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Itanium™

Major Phases of a Transaction

- **Arbitration Phase (ARB)**
  - **Arbitrate to use the bus**
- **Request Phase (REQ)**
  - **Start transaction: put the request (write, read) on the bus**
- **Snoop Phase (SNP)**
  - **Snoop results are put out**
- **Response Phase (RESP)**
  - **Transaction is concluded with a data transfer**

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Itanium™

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Itanium™

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Itanium™

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Pipelining

Time	1	2	3	4	5	6
transaction0	ARB					
transaction1						
transaction2						
transaction3						

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Pipelining

Time	1	2	3	4	5	6
transaction0	ARB	REQ				
transaction1		ARB				
transaction2						
transaction3						

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Itanium™

Pipelining

Time	1	2	3	4	5	6
transaction0	ARB	REQ	SNP	RESP		
transaction1		ARB	REQ	SNP	RESP	
transaction2			ARB	REQ	SNP	RESP
transaction3				ARB	REQ	SNP

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Itanium™ — Pipelining

Time	1	2	3	4	5	6
transaction0	ARB	REQ	SNP	RESP		
transaction1		ARB	REQ	SNP	RESP	
transaction2			ARB	REQ	SNP	RESP
transaction3				ARB	REQ	SNP

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Itanium™ — Pipelining

Time	1	2	3	4
	ARB	REQ	SNP	RESP

34

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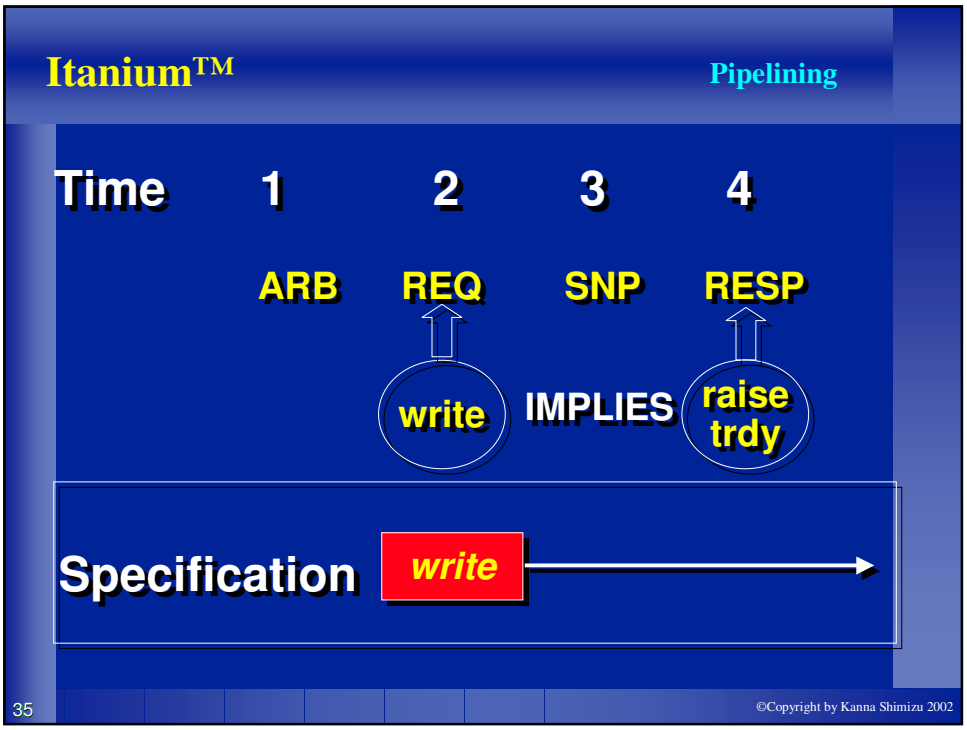
Itanium™
Pipelining
Time 1 2 3 4
ARB REQ SNP RESP
write
IMPLIES
raise trdy
Specification
write
35
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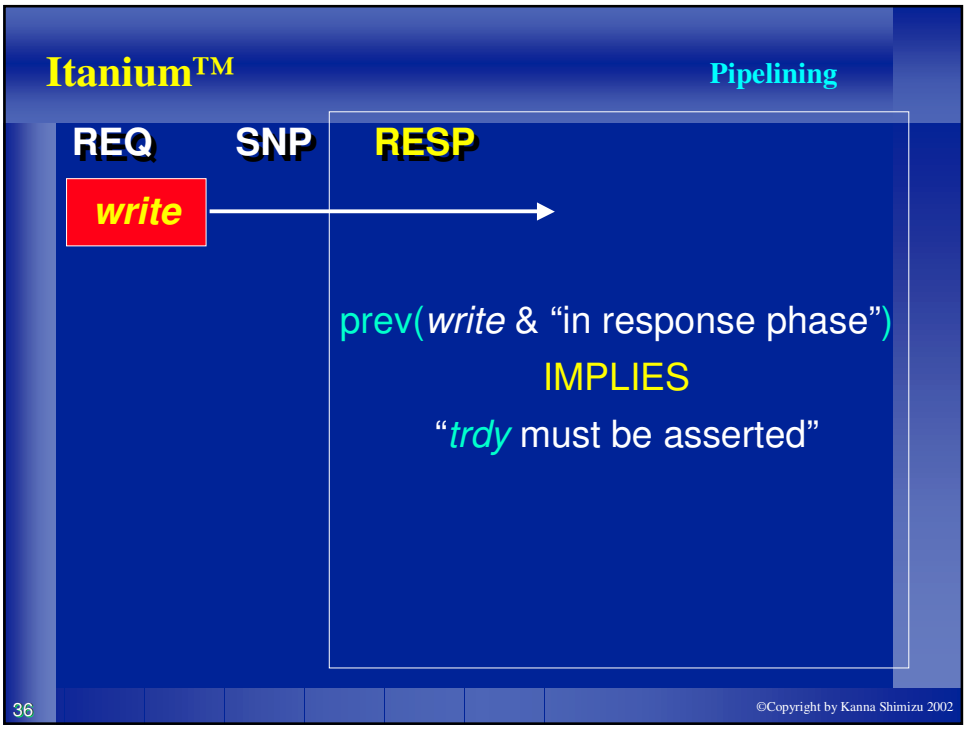
Itanium™
Pipelining
REQ SNP RESP
write
prev(write & "in response phase")
IMPLIES
"trdy must be asserted"
36
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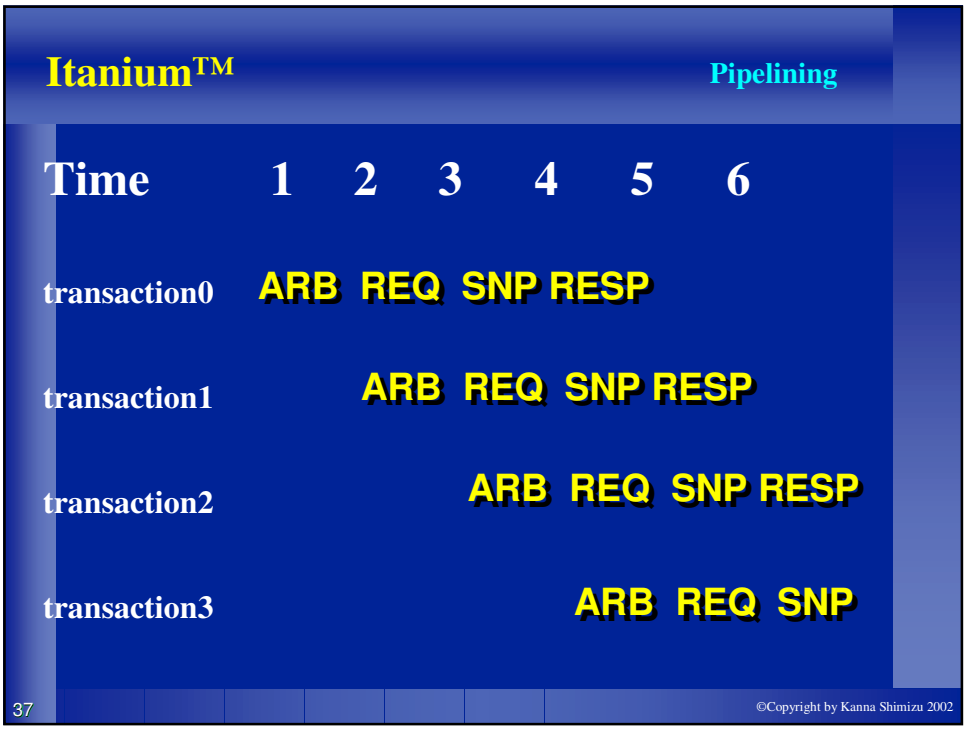
Itanium™
Pipelining
Time 1 2 3 4 5 6
transaction0 ARB REQ SNP RESP
transaction1 ARB REQ SNP RESP
transaction2 ARB REQ SNP RESP
transaction3 ARB REQ SNP
37
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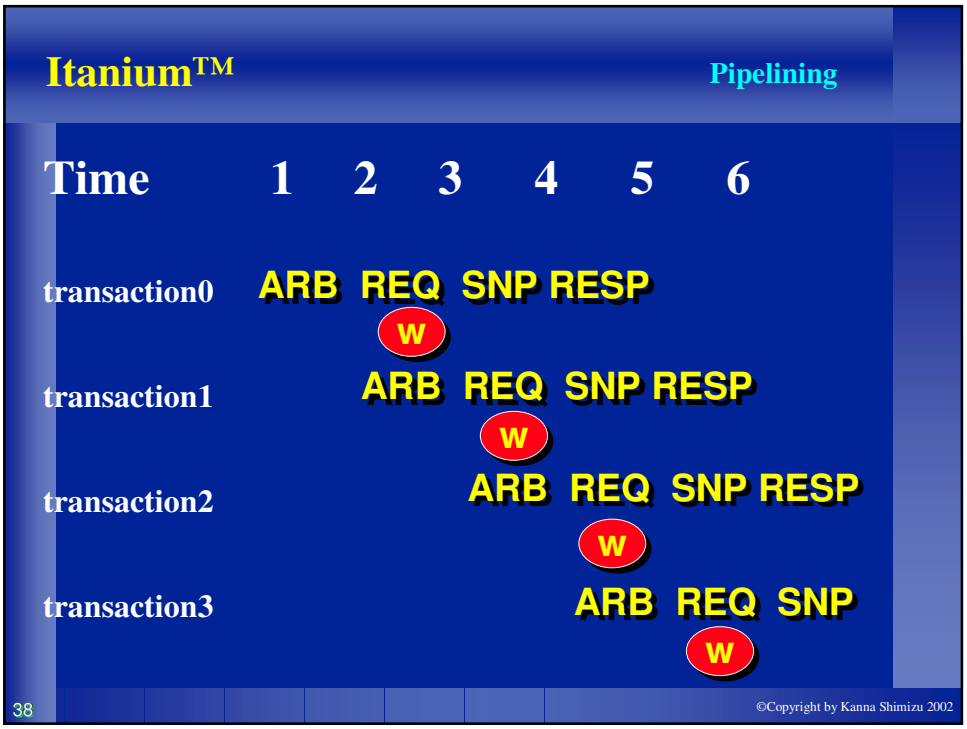
Itanium™
Pipelining
Time 1 2 3 4 5 6
transaction0 ARB REQ SNP RESP
W
transaction1 ARB REQ SNP RESP
W
transaction2 ARB REQ SNP RESP
W
transaction3 ARB REQ SNP
W
38
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Itanium™

Pipelining

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Pipelining

Multiple Instantiations

prev(*write* & "in response phase") IMPLIES "*trdy* must be asserted"

prev((RESP = 0) & write_*0*) IMPLIES "*trdy* must be asserted"

prev((RESP = 1) & write_*1*) IMPLIES "*trdy* must be asserted"

prev((RESP = 2) & write_*2*) IMPLIES "*trdy* must be asserted"

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Outline

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2. Specifying the Itanium™ processor bus protocol
3. Checking the protocol

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Deadlock Found in Protocol

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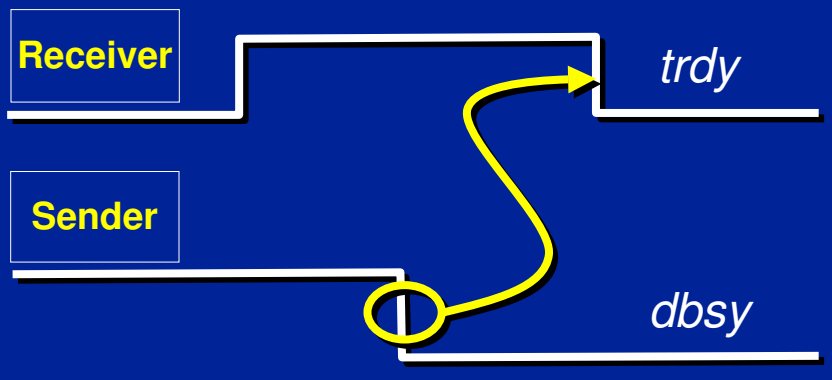
Normal Sequence



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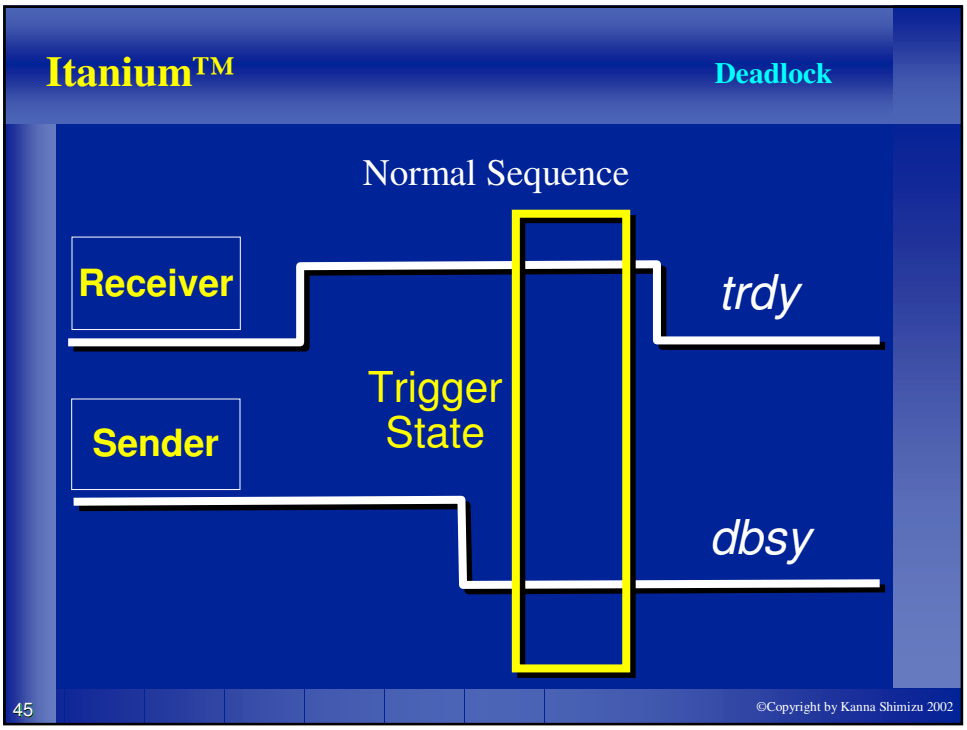
Itanium™
Deadlock
Normal Sequence
Receiver
Sender
Trigger State
trdy
dbsy
45
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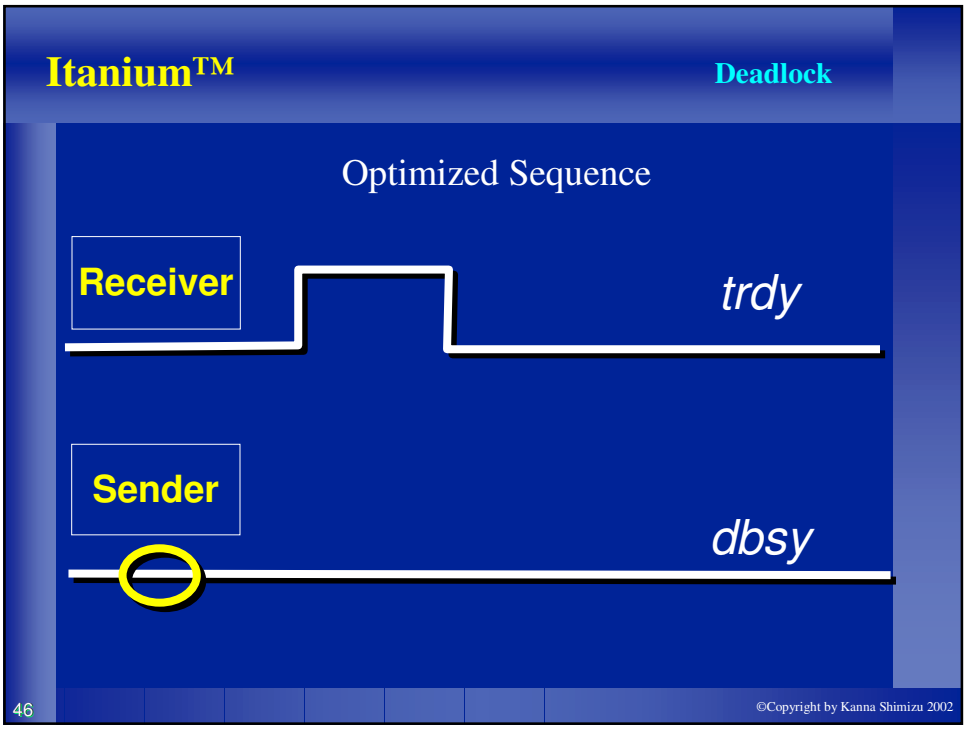
Itanium™
Deadlock
Optimized Sequence
Receiver
Sender
trdy
dbsy
46
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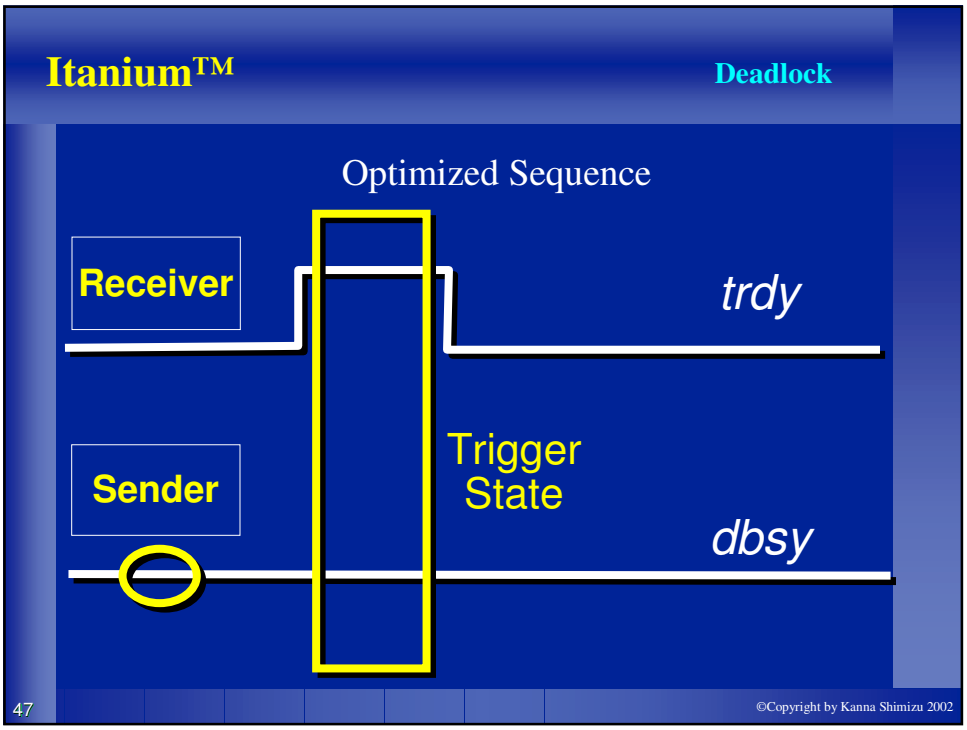
Itanium™
Deadlock
Optimized Sequence
Receiver
trdy
Trigger
State
Sender
dbsy
47
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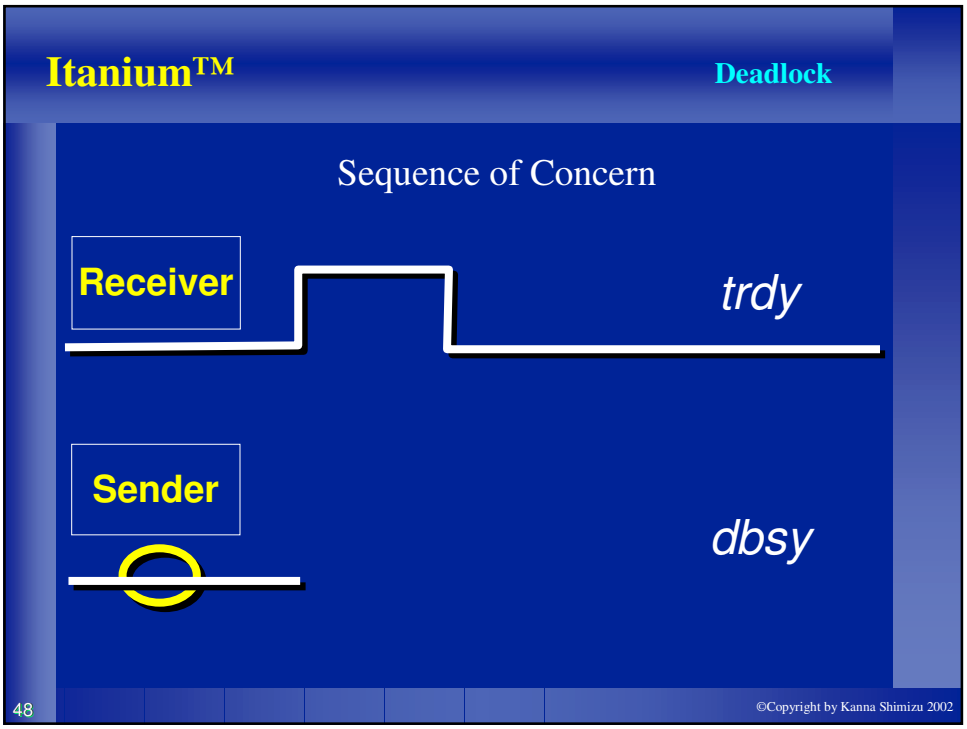
Itanium™
Deadlock
Sequence of Concern
Receiver
trdy
Sender
dbsy
48
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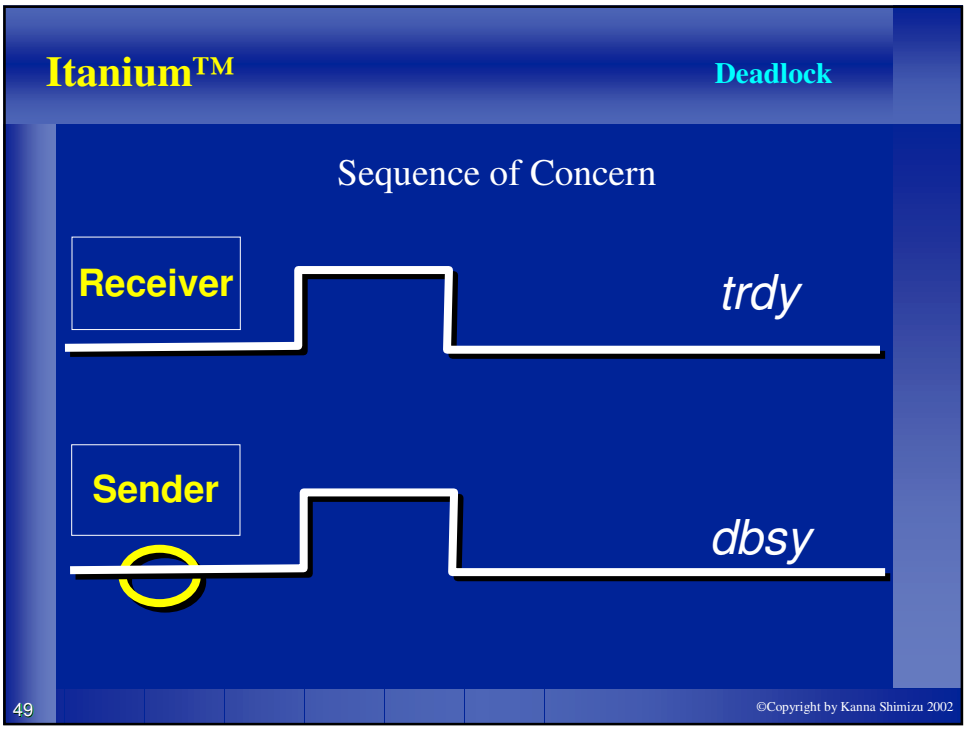
Itanium™
Deadlock
Sequence of Concern
Receiver
trdy
Sender
dbsy
49
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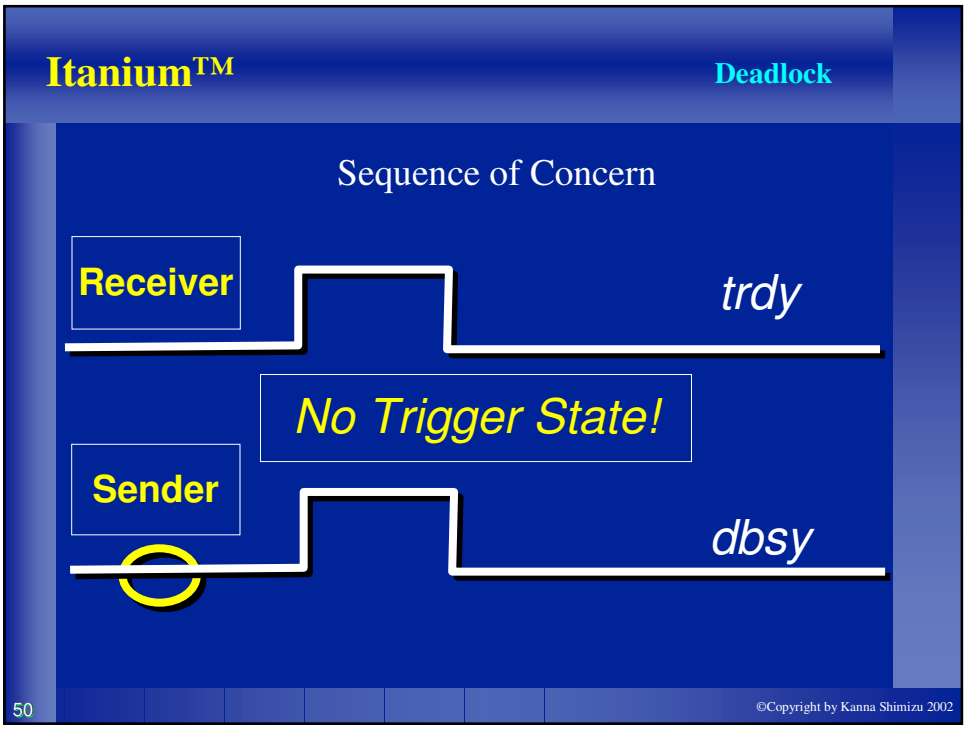
Itanium™
Deadlock
Sequence of Concern
Receiver
trdy
No Trigger State!
Sender
dbsy
50
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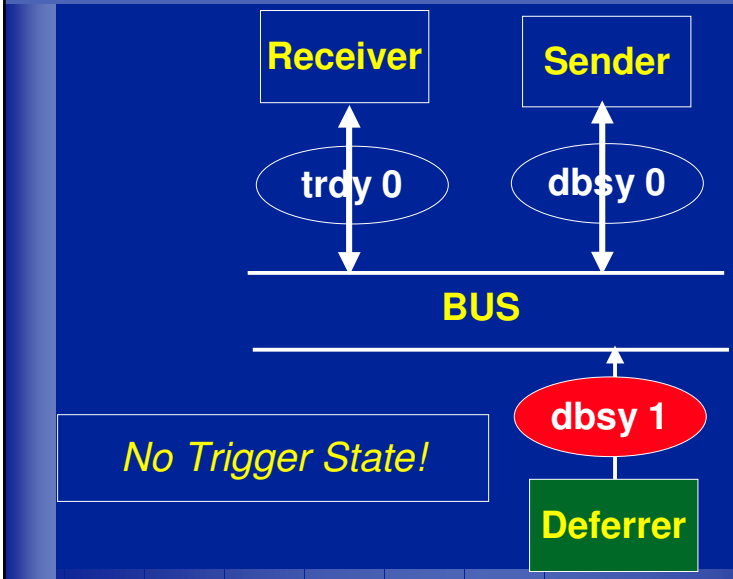

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- Consequences
  - Data transfer permanently blocked
  - Deadlock in some cases

Fixed

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Itanium™ Summary

- Experience specifying and checking
  - Two issues found with the protocol
    - Resulted in changes to the protocol
  - Formal specification written and debugged in two man-months
    - Partial description
    - Core protocol in 46 independent constraints

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Conclusion

1. Methodology
   - Simple yet effective
2. Specifying the Itanium™ bus protocol
   - Advanced, with pipelining
3. Checking the protocol
   - Issues discovered
   - Formal work fed back to standard rectification

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Future Directions

- Complete Specification
- Extract Useful Information
  - For synthesis
  - "Don't Care"s

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